REMARKS

Claims 1-10 remain in this application. Claims 1-10 have been amended, and new claims 11-14 have been added. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Versions with Markings to Show Changes Made.**" A request for continued examination is filed with this Response.

Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kochi et al. in view of Yoshida et al. Applicant respectfully traverses this rejection because the cited references, alone or in combination, do not disclose or suggest the timing adjustment means using a control signal other than the clear signal or the transfer signal (used in the operation of the operation means) in the timing adjustment, as now recited in independent claim 1.

As amended, claim 1 calls for the operation of operation means being based on at least one of a clear signal or a transfer signal, and outputting means for receiving the result of the operation of the operation means and outputting the result of the operation for each of the elements. Furthermore, claim 1 recites that the timing adjustment means uses a control signal other than the clear signal or the transfer signal in the timing adjustment.

It is stated in the Office Action that the claimed operation means is disclosed by the arithmetic operation output 50 in an embodiment of Kochi et al. shown in Fig. 19A. The Examiner, however, recognizes that this embodiment does not disclose the timing adjustment means, but asserts that this feature is disclosed in another embodiment shown in Fig. 12 of the reference. Briefly, Fig. 12 of Kochi et al. shows an arithmetic operation circuit block 801-A which has seven inputs that are connected to corresponding latch circuits 12-A.

Claim 1 now calls for the operation of the operating means to be based on at least one of the clear signal and the transfer signal. These features are not disclosed or suggested in the arithmetic operation output 50 shown in Fig. 19A of Kochi et al. Claim 1 further calls for the timing adjustment means to use a control signal other than the clear signal or the transfer signal, which is also not disclosed or suggested in Fig. 12 of Kochi et al. Moreover, even if the arithmetic operation output of Kochi et al. were to include the claimed clear signal and the transfer signal, the reference still would not disclose or suggest the timing adjustment means using a control signal other than the clear signal or the transfer signal of the operation means, as in the present invention.

The Yoshida et al. reference is cited in the Office Action as disclosing a plurality of arithmetic units for parallel processing. This reference also does not disclose or suggest the operation of the operation means being based on a clear signal and a transfer signal, or the timing adjustment means using a control signal other than the clear signal or the transfer signal. Thus, even if these references were combined, they still would not disclose or suggest the claimed operation means and the timing adjustment means as now recited in claim 1. For these reasons, claim 1 and its dependent claims 2-5 are allowable over Kochi et al. in view of Yoshida et al.

Independent claim 6 has also been amended to recite, in a method format, the features of the operating means and timing adjustment means as now described in claim 1. As such, claim 6 and its dependent claims 7-10 are also allowable for the same reasons given with respect to claim 1.

New independent claim 11 describes in part operation means which is operated based on at least a clear signal or a transfer signal. The operation of the operation means includes a plurality of modes, which are selected based on a control signal other than the clear signal or the transfer signal. As discussed above, the arithmetic operation output 50 of Kochi et al. does not disclose or suggest the clear signal or the transfer signal. Even assuming that the arithmetic operation output of Kochi et al. somehow discloses the clear signal or the transfer signal, it certainly does not disclose or suggest that the operation means includes a plurality of modes which are selected based on a control signal other than the clear signal or the transfer signal. Claim 12 describes in a method format features similar to those of claim 11. For these reasons, new independent claims 11 and 12 are allowable over Kochi et al. and Yoshida et al., alone or in combination.

New claims 13-15 depend from claim 1 and are allowable for the reasons given with respect to claim 1.

In light of the above, Applicants respectfully submit that claims 1-14 are both not anticipated and non-obvious over the art of record. Accordingly, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1-10 have been amended as follows:

1. (Twice amended) An image processing apparatus having an optical area in which a plurality of elements are disposed in a matrix, comprising:

light reception means for receiving light introduced into said elements of said optical area and photoelectrically converting the light;

~~arithmetic~~ operation means including a plurality of ~~arithmetic~~ operating units, each of which ~~arithmetically~~ operates a signal obtained for one of said elements by the photoelectric conversion by said light reception means in accordance with a predetermined rule, the operation of said operating means being based on at least one of a clear signal and a transfer signal;

outputting means for receiving a result of the operation of said operation means and outputting ~~a~~ the result of the ~~arithmetic~~ operation ~~of said arithmetic operation means~~ for each of said elements; and

timing adjustment means for adjusting a timing at which the result of the ~~arithmetic~~ operation is ~~to be outputted~~ output for each of said plurality of elements from said outputting means, said timing adjustment means using a control signal other than the clear signal or the transfer signal in the timing adjustment.

2. (Once amended) An image processing apparatus according to claim 1, wherein said ~~arithmetic~~ operation means includes storage means for successively storing a plurality of signals at different timings obtained by the photoelectric conversion.

3. (Once amended) An image processing apparatus according to claim 2, wherein said ~~arithmetic~~ operation means executes a comparison ~~arithmetic~~ operation for a combination of a plurality of ones of the signals stored in said storage means.

4. (Once amended) An image processing apparatus according to claim 3, wherein the comparison ~~arithmetic~~ operation includes an arithmetic operation for determining a maximum value or a minimum value of the signal.

5. (Once amended) An image processing apparatus according to claim 1, wherein said outputting means outputs results of ~~the~~ an arithmetic operation for each of the rows or the columns of said elements at a timing adjusted by said timing adjustment means.

6. (Twice amended) An image processing method for an image processing apparatus which has an optical area in which a plurality of elements are disposed in a matrix, comprising:

a light reception step of receiving light introduced into said elements of said optical area and photoelectrically converting the light;

an ~~arithmetic~~ operation step of ~~arithmetically~~ operating a plurality of signals in parallel obtained for each of said elements by the photoelectric conversion of the processing in the light reception step in accordance with a predetermined rule, the operation being based on at least one of clear signal and transfer signal;

an outputting step of receiving a result of the operation from the operation step and outputting ~~a~~ the result of the ~~arithmetic~~ operation ~~of the processing in the arithmetic~~ step for each of said elements; and

a timing adjustment step of adjusting a timing at which the result of the ~~arithmetic~~ operation is ~~to be outputted~~ output for each of said plurality of elements by the processing in the outputting step, said timing adjustment step using a control signal other than the clear signal or the transfer signal in the timing adjustment.

7. (Once amended) An image processing method according to claim 6, wherein the ~~arithmetic~~ operation step includes a storage step of successively storing a plurality of signals at different timings obtained by the photoelectric conversion.

8. (Once amended) An image processing method according to claim 7, wherein the ~~arithmetic~~ operation step executes comparison ~~arithmetic~~ operation for a combination of a plurality of ones of the signals stored by the storage step.

9. (Once amended) An image processing method according to claim 8, wherein the comparison ~~arithmetic~~ operation includes an arithmetic operation for determining a maximum value or a minimum value of the signal.

10. (Once amended) An image processing method according to claim 6, wherein the outputting means outputs results of ~~the~~ an arithmetic operation for each of the rows or the columns of said elements at a timing adjusted by the timing adjustment step.

New claims 11-15 have been added.